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a data processor for executing a predetermined graphic processing to generate graphic data to be stored in said memory;

output means for outputting said graphic data read out from said memory;

a memory controller for controlling data transfer between said memory and said data processor in accordance with a request from said data processor;

a first bus, having m (wherein m is an integer) bits width, connected between said memory and said memory controller, for transferring m bits of data in parallel; and

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a second bus, having n (wherein n is an integer, $n > m$) bits width, connected between said memory controller and said data processor, for transferring n bits of data in parallel;

wherein said memory controller comprises:

a storage for temporarily storing graphic data read out from said memory in successive groups of m bits of data during a predetermined period of time through said first bus,

means for forming n bits of data using said successive groups of m bits of data and supplying said n bits of data in parallel to said data processor through said second bus based on an indication from said data processor, and

a converter for converting said graphic data temporarily stored in said storage into serial data which is provided to said output means based on an indication from said data processor.

10. An apparatus according to claim 9, wherein said memory controller further comprises:

a multiplexer for outputting the n bits graphic data transferred from said data processor to said first bus having m bits width in a time shared fashion.

11. An apparatus according to claim 9, wherein said memory controller further comprises:

means for generating an address signal for accessing said memory plural times, in response to a signal for accessing said memory supplied from said data processor.

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12. An apparatus according to claim 9, wherein graphic data to be transferred to said memory controller through said first bus is read out from said memory plural times within a unit transfer time in a time shared fashion, based on an access signal to said memory designated by said data processor.

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13. An apparatus according to claim 12, wherein the graphic data transferred to said memory controller is supplied to said data processor through said second bus within a time longer than twice said unit transfer time.

14. A graphic processing apparatus comprising:
memory means for storing graphic data;

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data processing means for executing predetermined graphic processing to generate graphic data;

output means for outputting graphic data stored in said memory means;

a memory controller for controlling transfer of data between said memory means and said data processing means in response to a request from said data processing means;

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a first bus having an m-bit width (wherein m is an integer) and connected between said memory means and said memory controller, for transferring data of m bits in parallel; and

a second bus having an n-bit width (wherein n is an integer and $n > m$) and connected between said memory controller and said data processing means, for transferring data of n bits in parallel,

wherein said memory controller includes:

storage means for temporarily storing graphic data read out from said memory means successively in a predetermined period of time via said first bus,

means for applying said temporarily stored graphic data to said data processing means as n-bit parallel data based on an indication from said data processing means, and

converting means for converting said temporarily stored graphic data into serial data and outputting the serial data to said output means based on an indication from said data processing means.

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15. A graphic processing apparatus according to claim 14, wherein said memory controller includes multiplexer means for outputting n-bit graphic data transferred from said data processing means on said first bus having the m-bit width successively in a time-sharing manner.

16. A graphic processing apparatus according to claim 14, wherein said memory controller includes means for generating address signals for accessing said memory means plural times with respect to a signal for accessing said memory means applied from said data processing means.

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17. A graphic processing apparatus according to claim 15, wherein said memory controller includes means for generating address signals for accessing said memory means plural times with respect to a signal for accessing said memory means applied from said data processing means.

18. A graphic processing apparatus according to claim 14, wherein graphic data to be transferred to said memory controller via said first bus are successively read out plural times within a transfer unit time in a predetermined period of time on the basis of an access signal to said memory means designated by said data processing means.

19. A graphic processing apparatus according to claim 15, wherein graphic data to be transferred to said memory controller via said first bus are successively read out plural times within a transfer unit time in a predetermined period of time on the basis of an access signal to said memory means designated by said data processing means.

20. A graphic processing apparatus according to claim 18, wherein graphic data transferred to said memory controller are applied to said data processing means via said second bus within a time period more than two times said transfer unit time.

21. A graphic processing apparatus according to claim 19, wherein graphic data transferred to said memory controller are applied to said data processing means via said second bus within a time period more than two times said transfer unit time.

22. A graphic processing apparatus comprising:
memory means for storing graphic data, said memory means being accessed by using a row address and a column address;

data processing means for executing predetermined graphic processing to generate graphic data;

output means for outputting graphic data stored in said memory means;

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a memory controller for controlling transfer of data between said memory means and said data processing means in response to a request from said data processing means;

a first bus having an m-bit width (wherein m is an integer) and connected between said memory means and said memory controller, for transferring data of m bits in parallel; and

a second bus having an n-bit width (wherein n is an integer and $n > m$) and connected between said memory controller and said data processing means, for transferring data of n bits in parallel; and

wherein said memory controller includes:

means for reading out a plurality of graphic data at different column addresses at a same row address from said memory means via said first bus successively in a predetermined period of time,

means for applying said read-out graphic data to said data processing means as n-bit parallel data based on an indication from said data processing means, and

converting means for converting said read-out graphic data into serial data and outputting the serial data to said output means based on an indication from said data processing means.

23. A graphic processing apparatus according to claim 22, wherein said memory controller includes means for successively generating a plurality of column addresses on the

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basis of a signal for accessing said memory means applied from said data processing means.

24. A memory controller for controlling transference of data between a memory and a processor, said memory controller comprising:

m bit terminals for coupling to said memory, wherein successive groups of m bits of data is transferred through said m bit terminals between said memory and said controller by performing plural read operations within a memory cycle (where m is an integer);

n bit terminals for coupling to said processor, wherein n bits of data is transferred in parallel through said n bit terminals between said controller and said processor (where n is an integer and $n > m$);

storage for temporarily storing graphic data read out from said memory in successive groups of m bits of data during a predetermined period of time through said m bit terminals;

means for forming n bits of data by combining successive groups of m bits of data from said m bit terminals and supplying said n bits of data in parallel to said n bit terminals based on an indication from said processor; and

converting means for converting said graphic data temporarily stored in said storage into serial data which is supplied to output means, said output means outputs graphic